Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A method of manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

applying a first test stress to selected cells of the plurality of memory cells with a built-in self test~~, the first test stress~~ by performing a plurality of test sequences, wherein each of said test sequences includes a test pattern used with a plurality of conditions and the plurality of conditions are different between each of said test sequences ~~providing a stress level that is outside of a predetermined range~~;

identifying at least one weak memory cell;

repairing the at least one weak memory cell; and

applying a second test stress to the selected cells and the repaired cells with the built-in self test, the second test stress being different from the first test stress.

2. (Currently Amended) The method of claim 1, wherein the step of applying a first test stress further comprises the step of operating the memory cells with a timing that exceeds ~~a predetermined~~ an operational timing ~~range~~.

3. (Cancelled)

4. (Currently Amended) The method of claim 1, wherein the step of applying a second test stress includes the step of applying an operational timing ~~within a predetermined timing range~~.

5. (Currently Amended) The method of claim 1, further comprising the step of applying the second test stress by performing a plurality of test sequences, wherein each of said test sequences includes a test pattern used with a plurality of conditions and the plurality of conditions are different between each of said test sequences.

6. (Currently Amended) The method of claim 1, wherein the step of applying a first test stress includes the step of operating each memory cell with at least one tight timing, the at least one tight timing being less than ~~a predetermined~~an operational timing ~~range~~.

7. (Currently Amended) A method for testing during manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

applying a first set of timings to selected cells of the plurality of memory cells using built-in self test controls~~, the first set of timings being outside of a predetermined timing range~~;

testing the selected cells using the first set of timings in a plurality of test sequences, wherein each of said test sequences includes a test pattern used with a plurality of conditions and the plurality of conditions are different between each of said test sequences;

identifying weak memory cells;

repairing the weak memory cells;

applying a second set of timings different from the first set of timings to the selected cells and the repaired cells using the built-in self test controls; and

testing the selected cells and the repaired cells using the second set of timings.

8. (Original) The method of claim 7, wherein the first set of timings provides at least a first stress to the cells and the second set of timings provides at least a second stress to the cells.

9. (Currently Amended) The method of claim 8, wherein the second set of timings tests the memory cells ~~within the predetermined~~at an operational timing ~~range~~.

10. (Currently Amended) The method of claim 8, wherein the first set of timings tests the memory cells at timings that are faster than ~~the predetermined~~an operational timing ~~range~~.

11. (Previously Presented) The method of claim 8, wherein the at least the first stress includes two or more stresses and the at least the second stress includes two or more further stresses, the method further comprising the steps of using the first set of timings to provide

the two or more stresses to the cells and using the second set of timings to provide the two or more further stresses to the cells.

12. (Currently Amended) A method of manufacturing a device having embedded memory including a plurality of memory cells, the method comprising the steps of:

(a) providing a first plurality of timings and a second plurality of timings to built-in self test controls, the first plurality of timings being different from the second plurality of timings~~, the first plurality of timings being outside of a predetermined timing range~~;

(b) applying at least one of the first plurality of timings to selected cells using the built-in self test controls by performing a plurality of test sequences, wherein each of said test sequences includes a test pattern used with a plurality of conditions and the plurality of conditions are different between each of said test sequences;

(c) identifying failed memory cells;

(d) repairing the failed memory cells; and

(e) repeating steps (b) to (d) by applying additional selected ones of the first plurality of timings to the cells.

13. (Original) The method of claim 12 further comprising the step of (f) applying at least one of the second plurality of timings to each of the cells using the built-in self test controls.

14. (Original) The method of claim 13 further comprising the step of (g) repeating step (f) by applying additional selected ones of the second plurality of timings to each of the cells.

15. (Currently Amended) A device for testing an embedded memory having a plurality of memory cells during manufacture of the embedded memory, the device comprising:

a first delay circuit comprising:

a first timer for applying a plurality of timings to the memory cells, the plurality of timings including an operational timing mode ~~within~~ at a predetermined level~~timing range~~, a plurality of relaxed timing modes that exceeds the predetermined timing ~~range~~ level and a plurality of tightened timing modes that is less than the predetermined timing ~~range~~level, and

a second timer for modifying at least one of the plurality of timings;

a second delay circuit coupled to the first delay circuit for modifying at least one of the plurality of timings to provide a timing that exceeds the plurality of relaxed timing modes; and

a logic circuit for testing the memory cells by applying the at least one of the plurality of timings to the memory cells.

16. (Original) The device of claim 15, further comprising a sensor coupled to the memory cells for determining whether the memory cells failed the testing; and a repair component for repairing failed cells.

17. (Cancelled)

18. (Previously Presented) The device of claim 15, wherein the first and second timers are located in at least one area of the embedded memory.

19. (Original) The device of claim 15, wherein the embedded memory includes a built-in self test for controlling the testing for determining whether any memory cells failed the testing.

20. (Original) The device of claim 19, wherein the embedded memory includes a built-in self repair for repairing failed memory cells.

21. (Previously Presented) The method of claim 1, further comprising the step of:

rejecting the embedded memory when at least one failed memory cell is identified from the applied second test stress.

22. (Currently Amended) The method of claim 1, wherein the step of applying the first test stress further comprises the step of operating the memory cells with a first timing that is outside of a predetermined timing ~~range~~ value and the step of applying the second test stress further comprises the step of operating the memory cells with a second timing that is different from the first timing.

23. (Previously Presented) The method of claim 7, further comprising the step of:

rejecting the embedded memory when at least one failed memory cell is identified from the second set of timings.

24. (Previously Presented) The method of claim 13, step (f) further comprising:

rejecting the embedded memory when one or more further failed memory cells are identified from the applied at least one of the second plurality of timings.